

Ultrasound Brain Imaging, Drive Circuitry

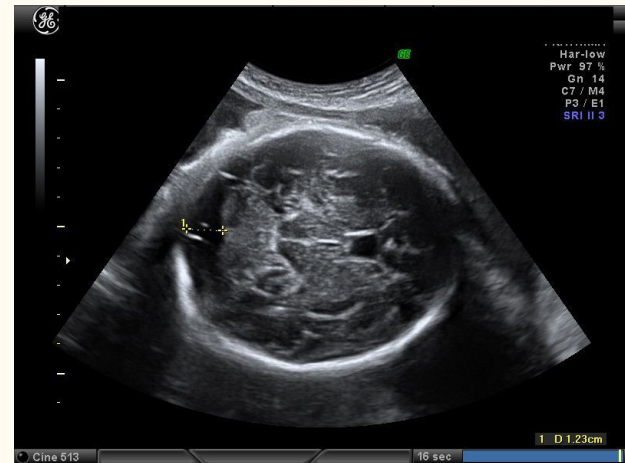
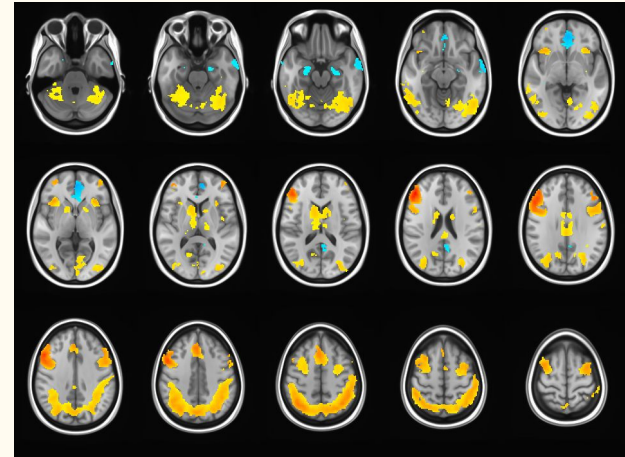
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Team Information

- Client and Faculty Adviser Info
 - Dr. Timothy Bigelow
- DEC1619 Team Members
 - Miguel Mondragon, Team Leader and Communications
 - Zechariah Pettit, Webmaster
 - Honghao 'Tom' Liu, Key Concept Holder

Brain Imaging, Technology

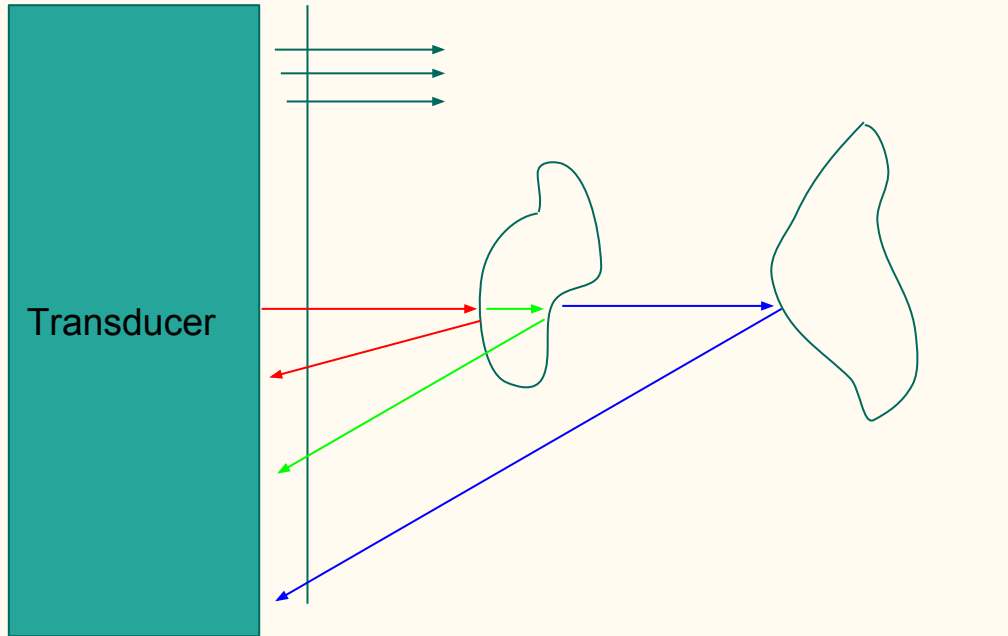
- fMRI, Magnetic Resonance Imaging
 - Uses a strong and static magnetic field on the brain.
 - Measures energy after field is removed.
 - Energy difference show blood oxidationation levels which can be used to create an image.
 - Effective imaging technique but expensive.
 - Not the right fit for some patients.
- Ultrasound Imaging
 - Transmits ultrasonic pulses from a transducer.
 - Measures energy and time for from the returning signals.
 - Has potential to be effective and less expensive, but requires specialized hardware.



Ultrasound Imaging

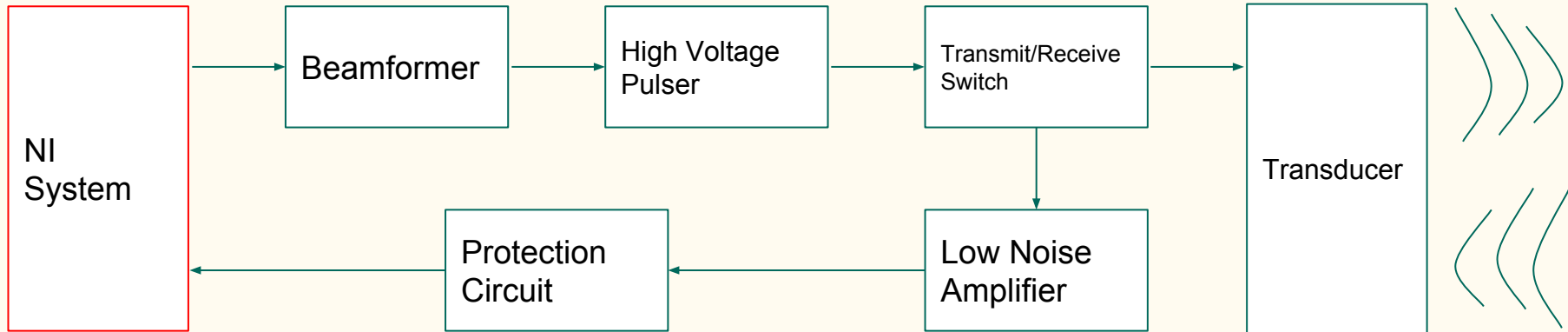
- A number of pulse signals with variable phase and voltage amplitude are transmitted through a transducer
- The signal is emitted through the transducer as a soundwave and then reflected.
- The time difference between sending and receiving a signal is then used to produce an image.
- The energy level of the receive signal can be used to determine object density.

Ultrasound Imaging



Project Approach, NI System

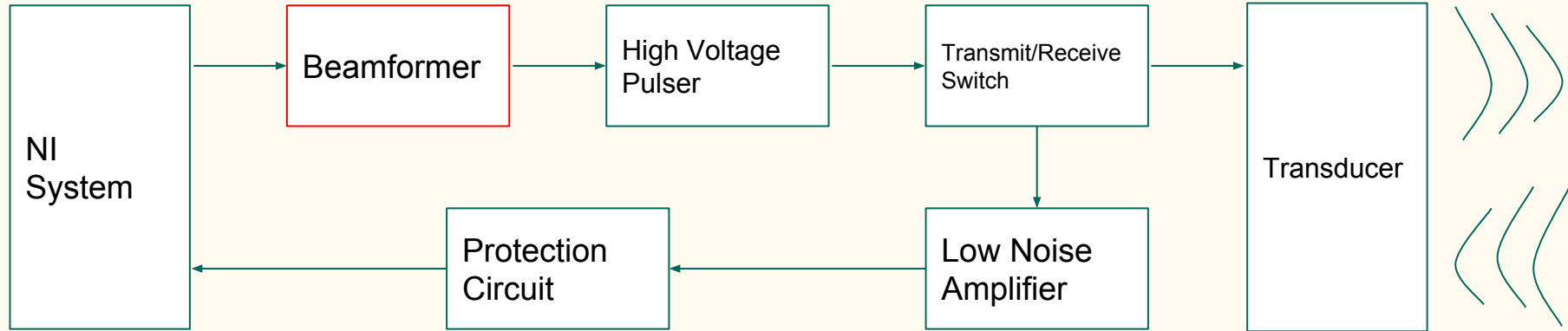
First the NI PXI Hardware, selected by Dr. Bigelow, serves as serial programmer to perform the computational needs of the system.



Project Approach, Beamformer

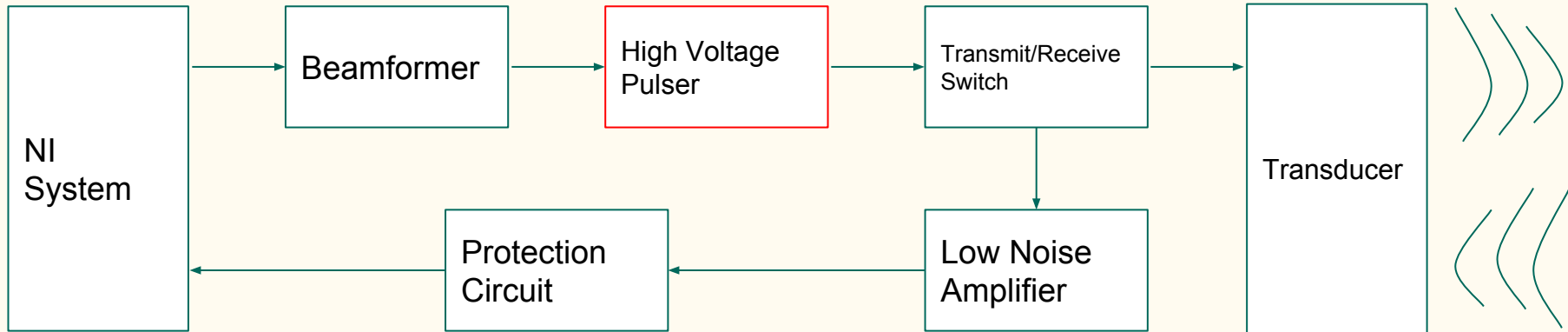
The beamformer determines the necessary signals to interface with the object being scanned and produces the initial signals based upon these needs.

In the case of this design the beamformer is in part controlled by the NI system and partially by our project's hardware.



Project Approach, High Voltage Pulser

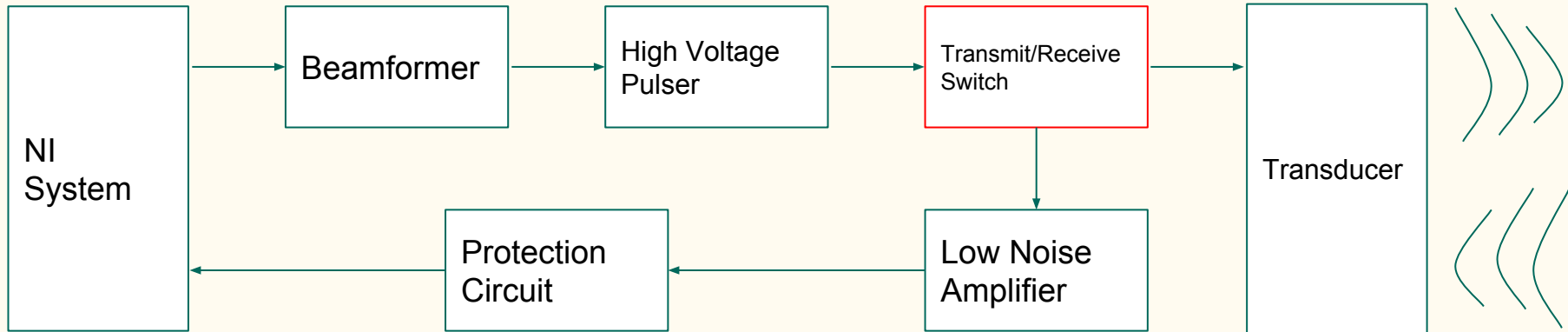
After receiving control signal from beamformer outputs a variable phase controlled and voltage amplified set of pulses to the transducer.



Project Approach, T/R Switch

Serves as a protection circuit for the transducer circuitry.

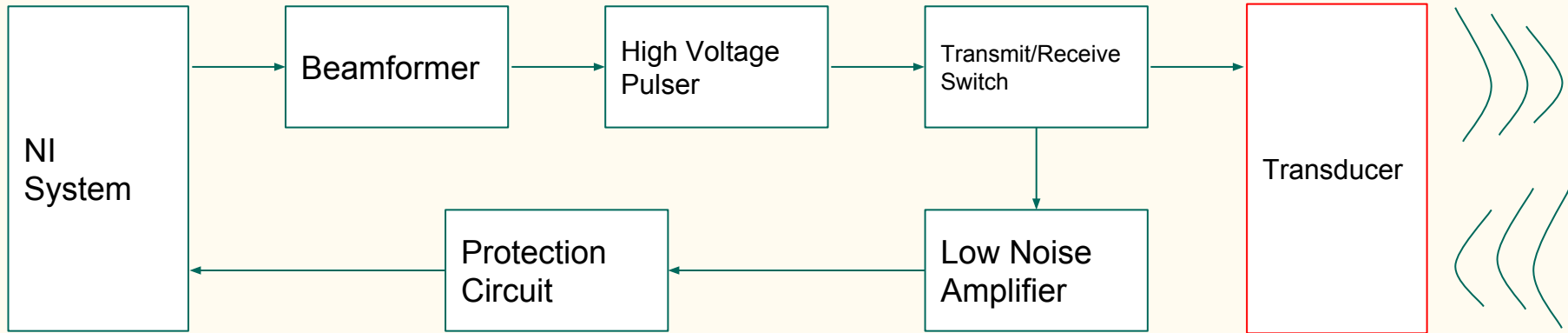
Serves as switch to differentiate between the transmission signal and the received signal by the transducer.



Project Approach, Transducer

A 512 channel linear array that converts the high voltage pulses into ultrasonic wave for imaging.

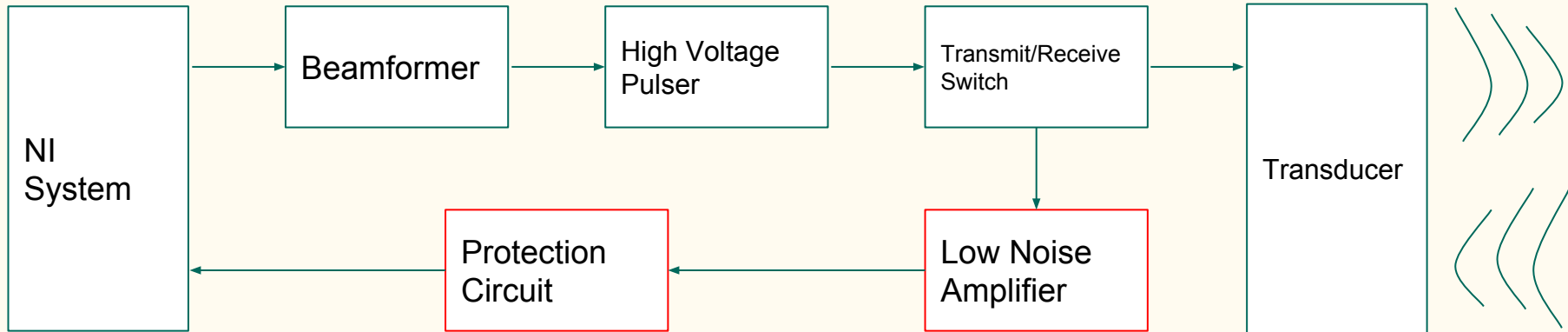
Transducer then receives the returned signals that then head to the LNA for processing.



Project Approach, Receive Circuitry

Received signal then goes through a low noise amplifier and then proceeds to another protection circuit that limits the signals to 2 Vpp.

Signal then proceeds to the NI Receive System.

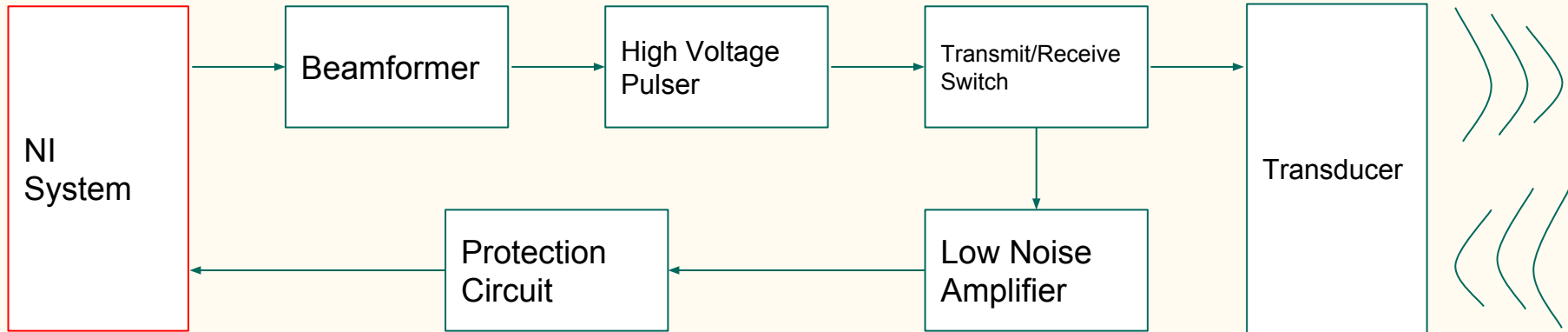


Project Approach, NI Receive System

Received signals then proceed to the NI-5752 module.

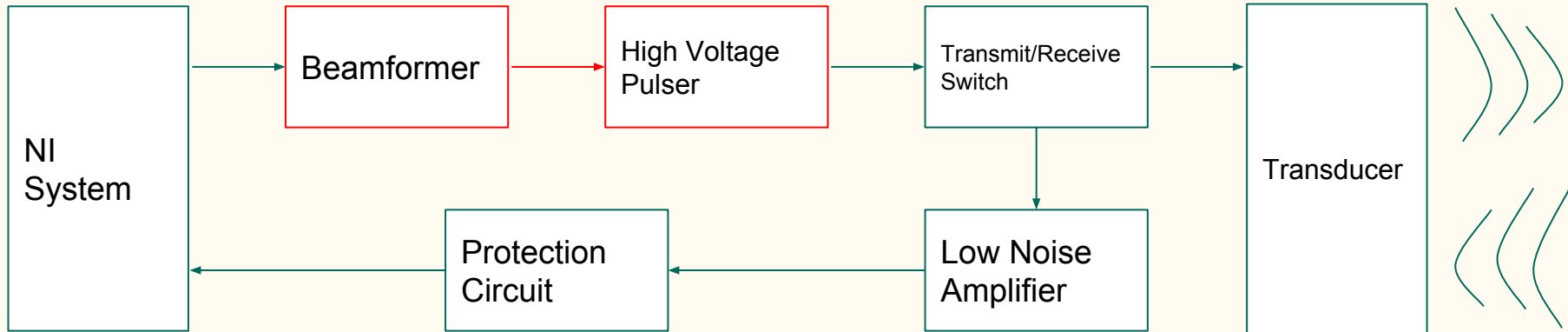
Signals are converted from analog to digital for processing.

Signal processing produces a B-mode or 2D image image with density mapping.



Problem Statement

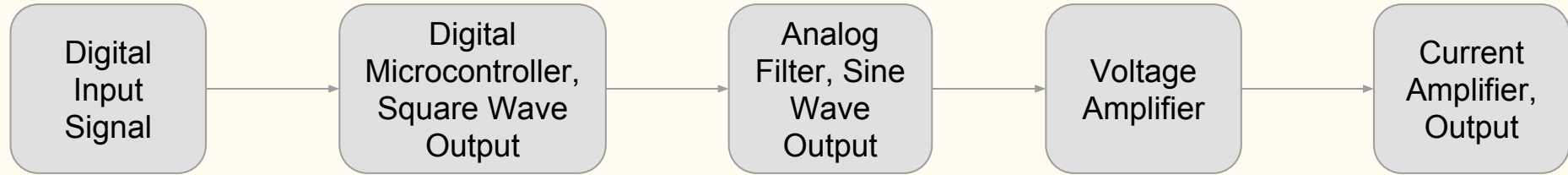
Our group has been tasked with creating the drive circuitry for the transmit side of the device, in particular beamformer and high voltage pulser, which will produce the signals sent to the transducer to be emitted as ultrasonic pulses.



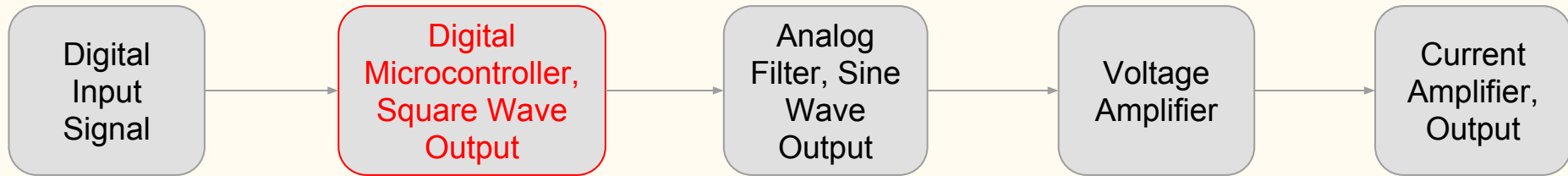
Functional Requirements

- A microcontroller to duplicate the input signal and apply individual phase control on maximum 8 PWM outputs.
- A digital to analog converter for these PWM signals.
- Filtering to reduce the square to a sinusoidal waveform.
- Filtering to prevent $>1.5\text{Mhz}$ signals.
- Amplification up to 32V.
- Transmit 8 channels of final sinusoidal signals.

Block Diagram



Digital Microcontroller



TI C2000 LaunchPad Microcontroller

- Generate simulated initial PWM input signal at various frequency and duty cycle.
- On board microcontroller has a 60 MHz clock frequency, target output frequency is 1.5 MHz.
- Compute delay digit based on command from TI CCS
- Transmit compiled code to the LaunchPad through USB
- Apply phase delay based on calculation above.
- Output phase delayed PWM signals with default 3.5V DC voltage.

Individual Phase Control Approach

- Initially we constructed a Simulink model on MATLAB to convert the digital input to analog sinusoidal first then apply phase delay.
- Relatively high frequency of the input digital signal bring a high noise on the DAC output.
- Approach of trying to connect TI LaunchPad with Simulink through USART failed, because Simulink failed to access random memory address on-board
- Finally by using on-board JTAG to transmit phase delay command through USB succeed

Individual Phase Control Solution

- Using TI ePWM mode on C2000 LaunchPad we have successfully applied phase control to duplicated input signal.
- Base on clock frequency of the microcontroller, we can choose our own reference signal with our choice of frequency and duty cycle.
- Delay individual signal base on the calculated digit for given phase.
- Output delayed signal using 'up-down' mode through on-board pin.
- All output signal has same 3.5V DC voltage.

PWM Phase Control Results

Pre-set reference frequency

- 10 KHz for clear image

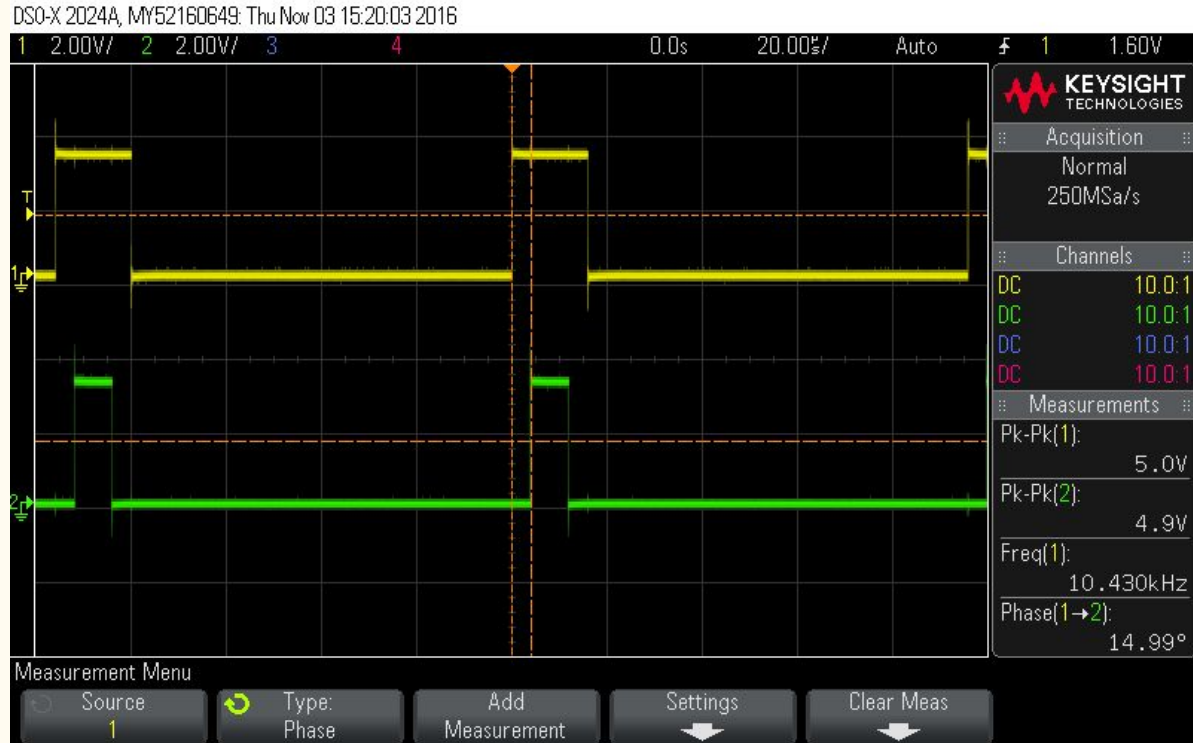
Various duty cycle

Channel 1

- 20%

Channel 2

- 10%

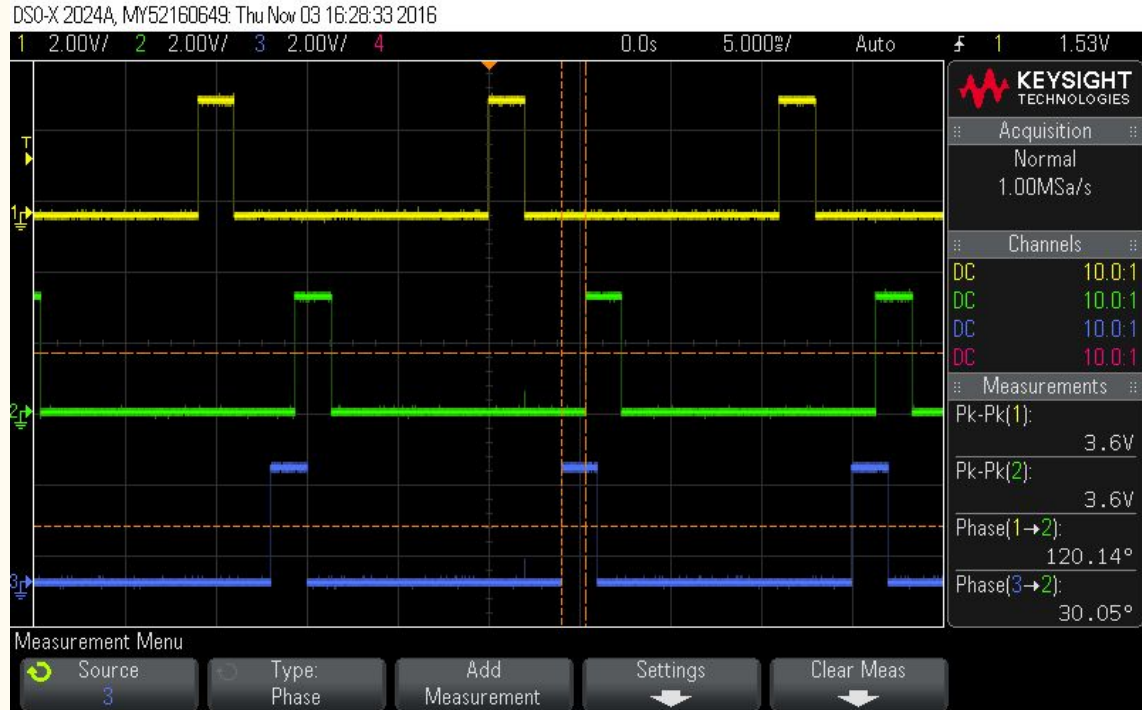


PWM Phase Control Results

Sample output

90 and 120 degree phase shift

Compare to reference signal



DAC Filter



High Frequency DAC Filter

Primary goal is the conversion of a square to an approximate sine wave. A digital to analog conversion.

Next is the ability to function under a wide range of duty cycles for variable voltage.

Attempts to reduce or eliminate circuit noise and settling time should be made.

Finally the circuit should filter out unexpectedly high frequencies.

Expect input signal of 1.5Mhz with 0V to 3.5V pulse width modulated square wave..

DAC Filter, Solution

The decided upon solution was an active lowpass filter followed by a passive high-pass filter to filter out any remaining DC signal.

A gain of 1.5 V/V was set so that at a -3dB frequency of 1.5Mhz the gain would be approximately 1 V/V with all frequency exceeding 1.5Mhz having voltages reduced.

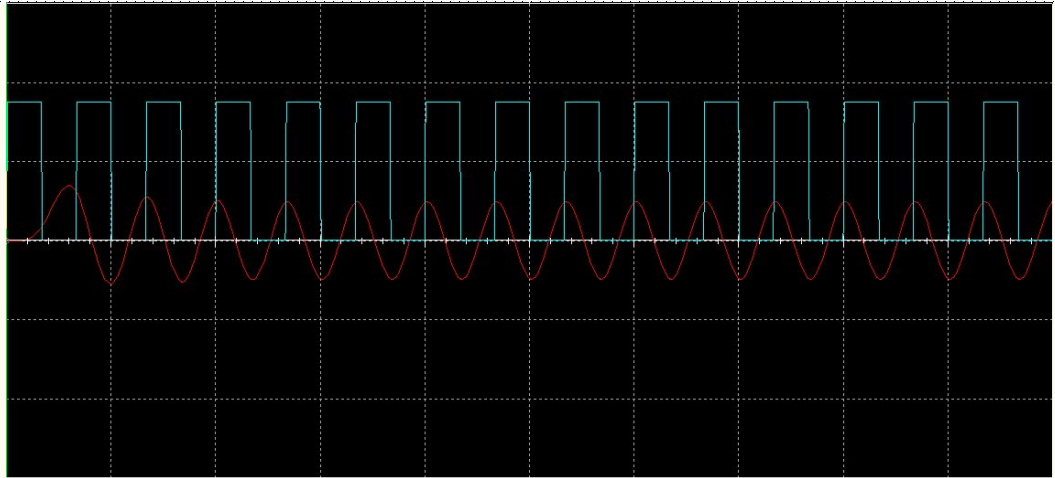
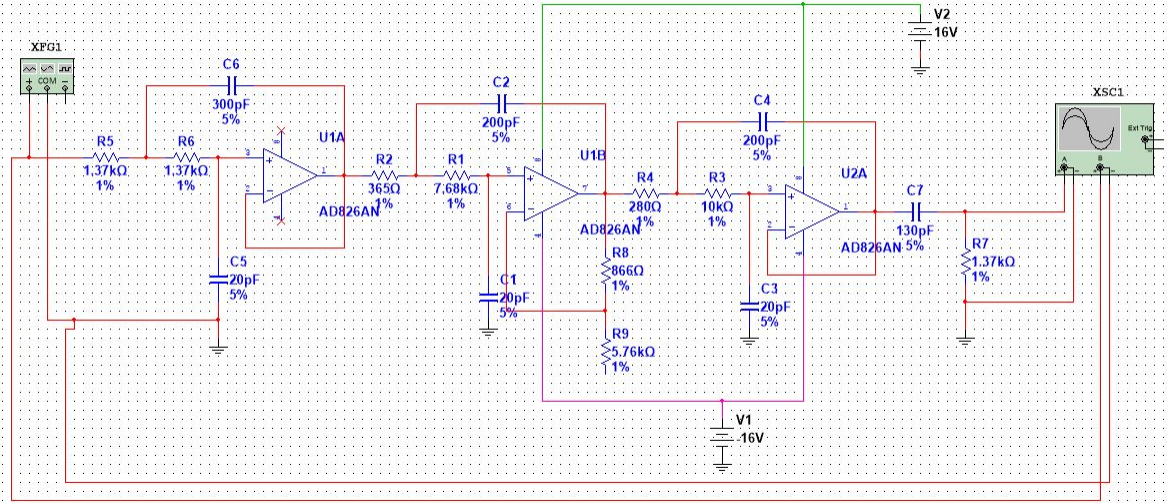
The filter design itself is a 6th order Butterworth filter with Sellen-Key filter circuits.

DAC Filter, Challenges

- DC Offset when using $<50\%$ duty cycle.
 - Implementation of high pass filter.
- Voltage losses due to duty cycle changes.
 - Implementation of a 4 V/V voltage gain for ideal results at 10% duty cycle.
- Multisim ran into excessive difficulties when attempting to simulate the filter circuits with input duty cycles under 30% .
- As the duty cycle percentage was lowered the ability to receive clear and stable signals became more difficult.
 - Operational amplifier and filter gain effects had to adjusted to allow the widest range of duty cycles.
- Excess noise generated by both the input frequency and the passive components of the circuit.

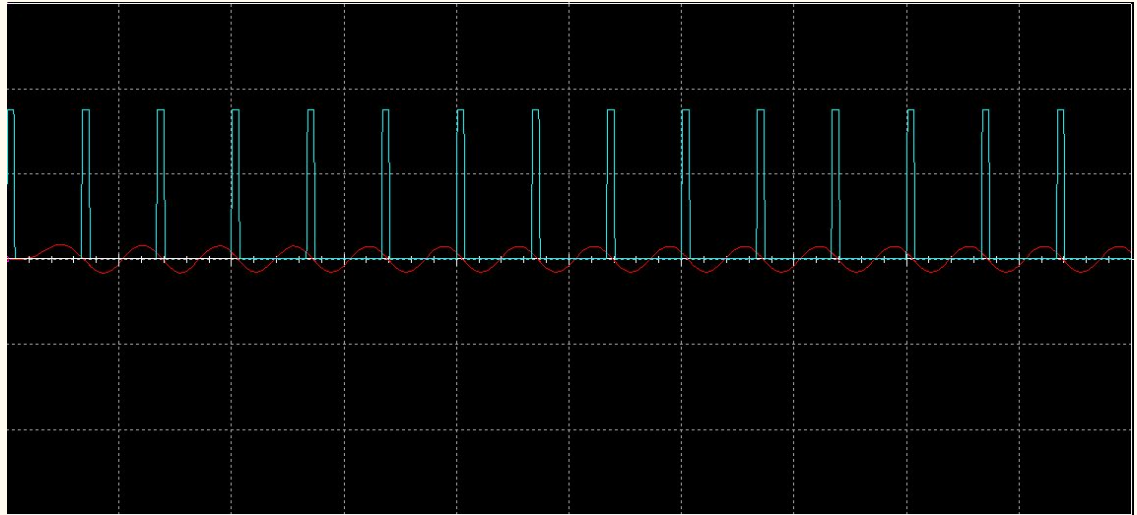
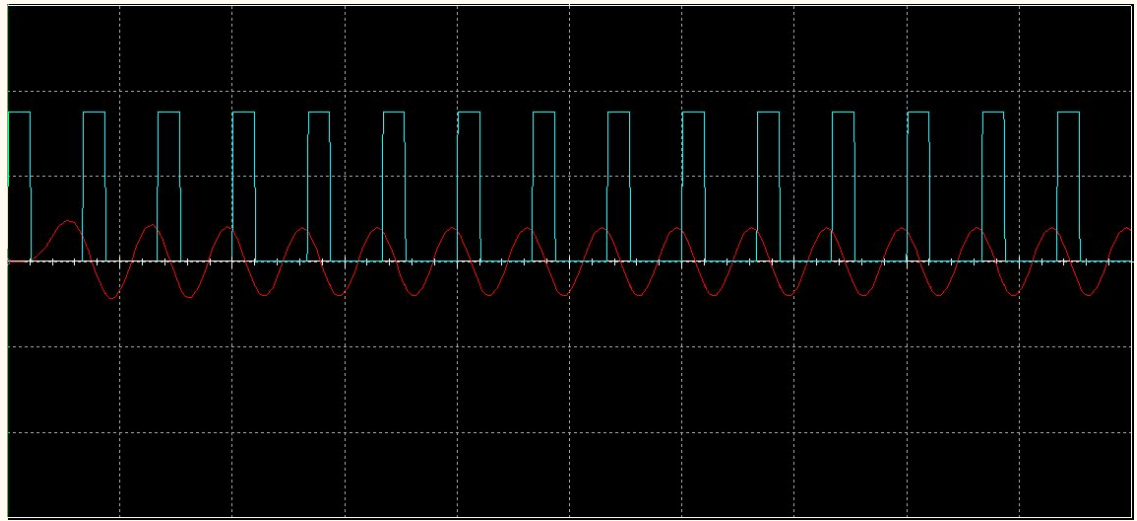
DAC Filter, Simulation Results

- Circuit is a 3 stage Sallen Key, 6th order butterworth filter.
- With a gain of 1.5 V/V and the desired filter limitation set by the lowpass filter the output has approximately a 1V/V output at the expected frequency of 1.5Mhz
- Output signal (red) shown below vs the input signal (green) a 3.5Vpp, 1.5Mhz, square wave at 50% duty cycle.
- The duty cycle has an impressive effect on the end voltage gain.



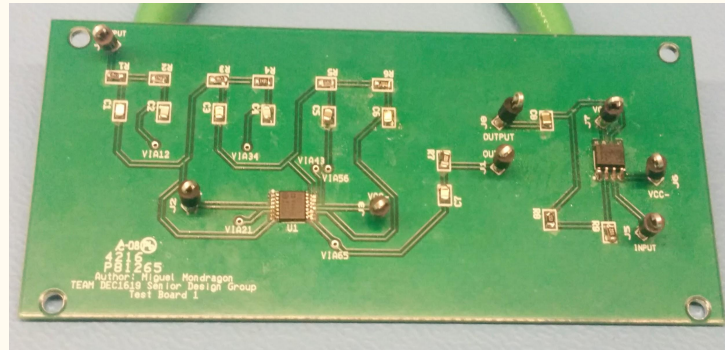
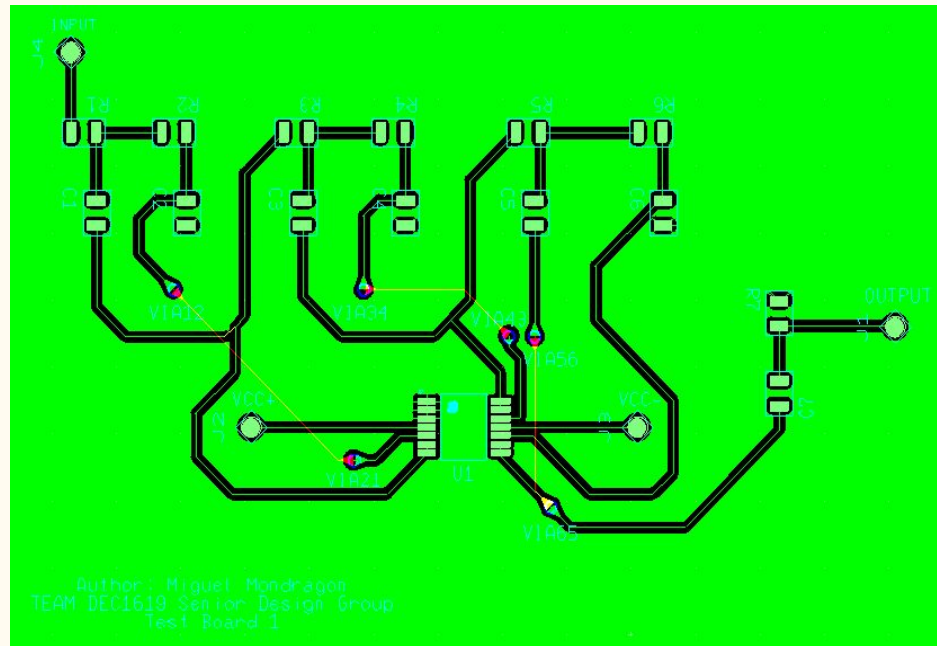
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DAC Filter, Test Board Results

- Based on the initial filter design at the end of Spring of 2016.
- Tested with a function generator signal and measured with an oscilloscope.
- First test resulted in a short lived sinusoidal signal with high noise. Second test resulted in an immediately burned out opamp.
- Result was due to either capacitive load exceeding op amp's parameters or initial voltage spike.
- In addition the operational amplifier used for this design is no longer available for purchase.



Power Amplifiers



Voltage Amplifier Challenges

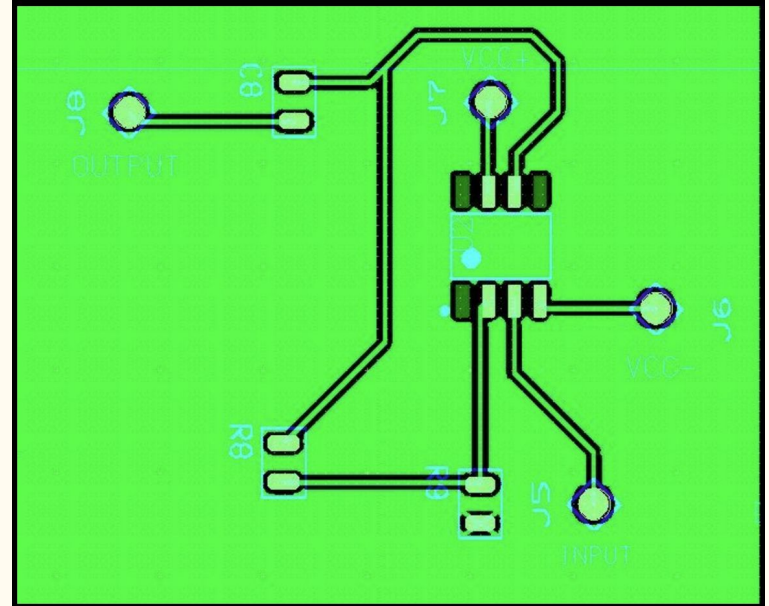
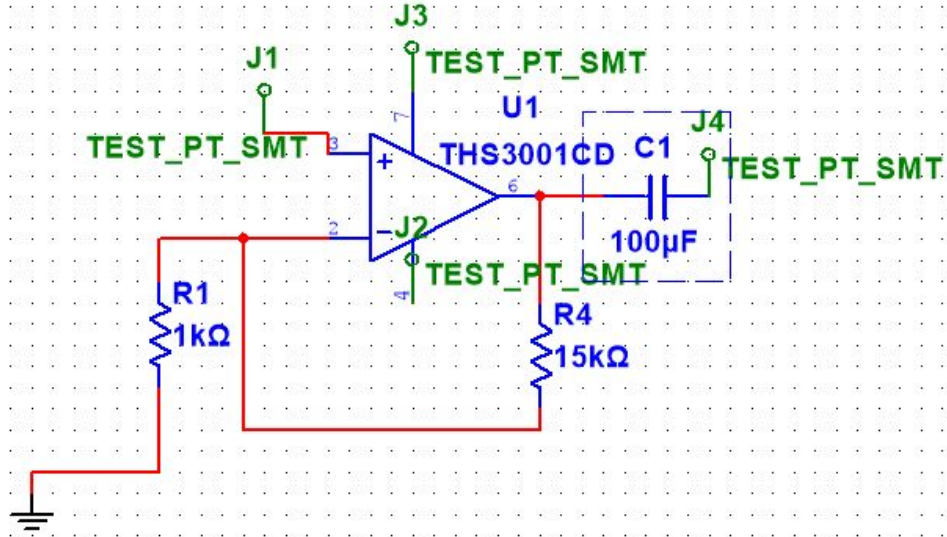
- Finding an amplifier
- Attempting to reach 50V with (OPA4548)
- Settling to 30V due to expense and limitation on parts

Voltage Amplifier Solution

Single channel voltage amplifier powered by high-speed TI THS3001 Op Amp

- 420-MHz Bandwidth
- THD = -96 dBc at $f = 1$ MHz
- -0.02° Differential Phase
- 6500-V/ μ s Slew Rate
- Output Current = 100 mA
- VCC = ± 16 V

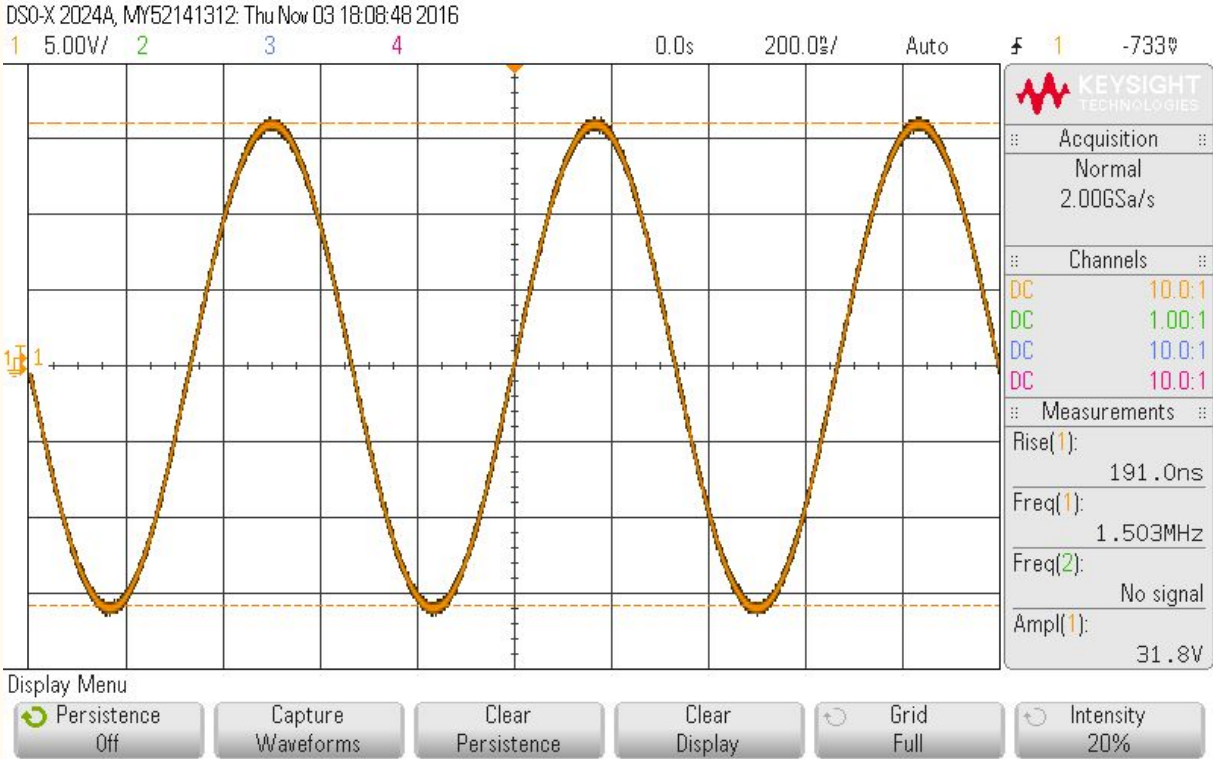
Voltage Amplifier



Voltage Amplifier Measured Result

2Vpp input

Gain = 15.9



Current Amplifier Solution

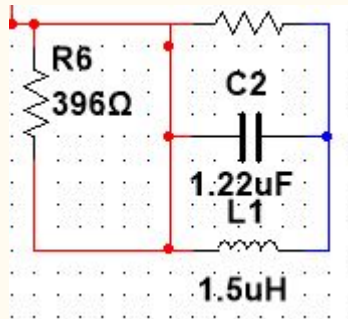
MJL3281A (NPN) and MJL1302A (PNP)

- NPN/PNP Gain Matching within 10% from 50 mA to 5 A
- High frequency for high amplifier bandwidth
- Exceptional Safe Operating Area for reliable performance at higher powers
- Excellent Gain Linearity for accurate reproduction of input signal

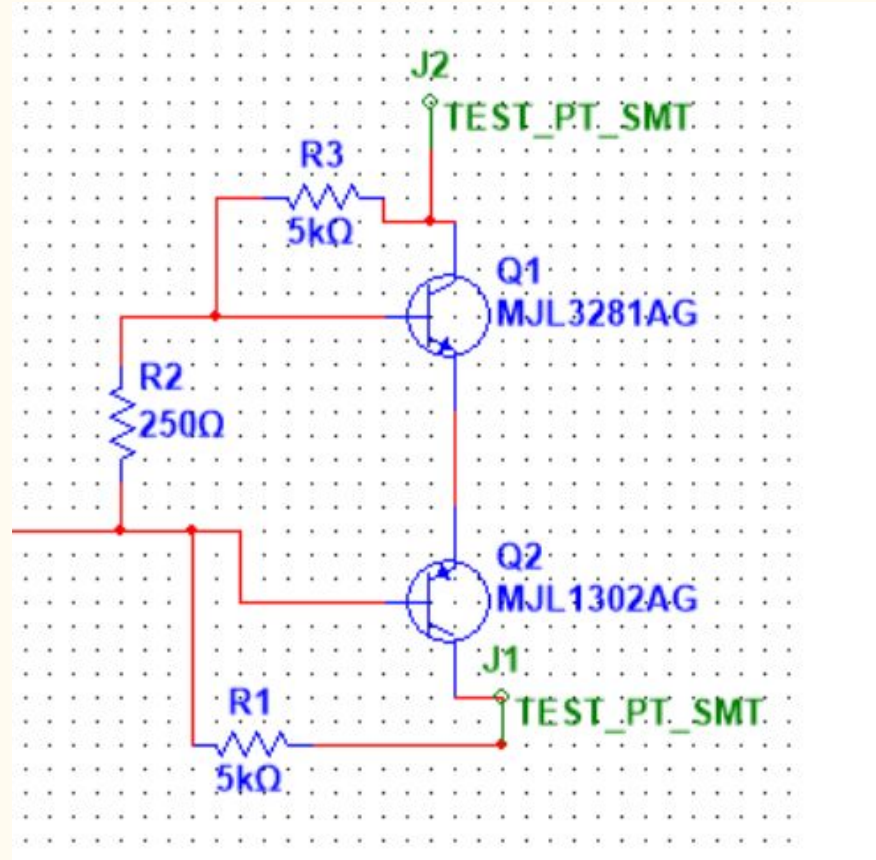
Current Amplifier

R2 sets bias

Designed to drive load with 5A



Equivalent impedance of transducer

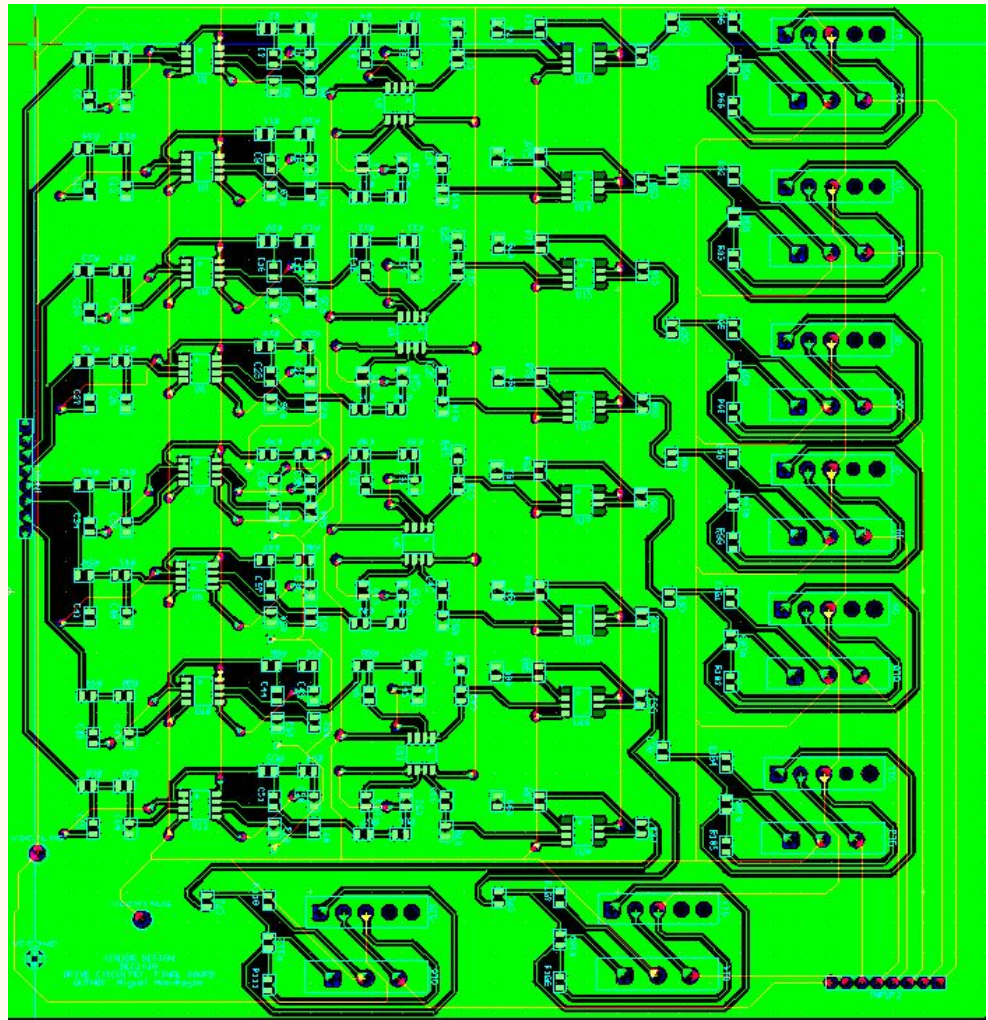


Testing Plan

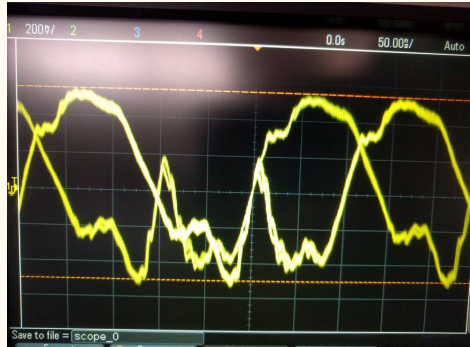
1. Conceptualize initial designs.
2. Simulate digitally with Multisim.
3. Select and test complex parts of design.
4. Create and test designs with physical PCB.
5. When encountering design flaws, determine origin of failure then re-conceptualize based on the failure.
6. Repeat Process.

Results

- TI C2000 LaunchPad performed as designed, delivering stable and accurate reference signals, as well as controlled phase delay and duty cycles.
- The DAC Lowpass Filter segment is working as intended from a simulation perspective.
- Voltage amplifier is functional in both simulation and physical perspective.
- Current amplifier is functional in simulation.
- Final PCB combining these elements has been prepared.
- Initial testing result of final PCB resulted in destruction of voltage amplifier IC's.
- Results most likely due to harmonics of passive component elements effecting source voltages.



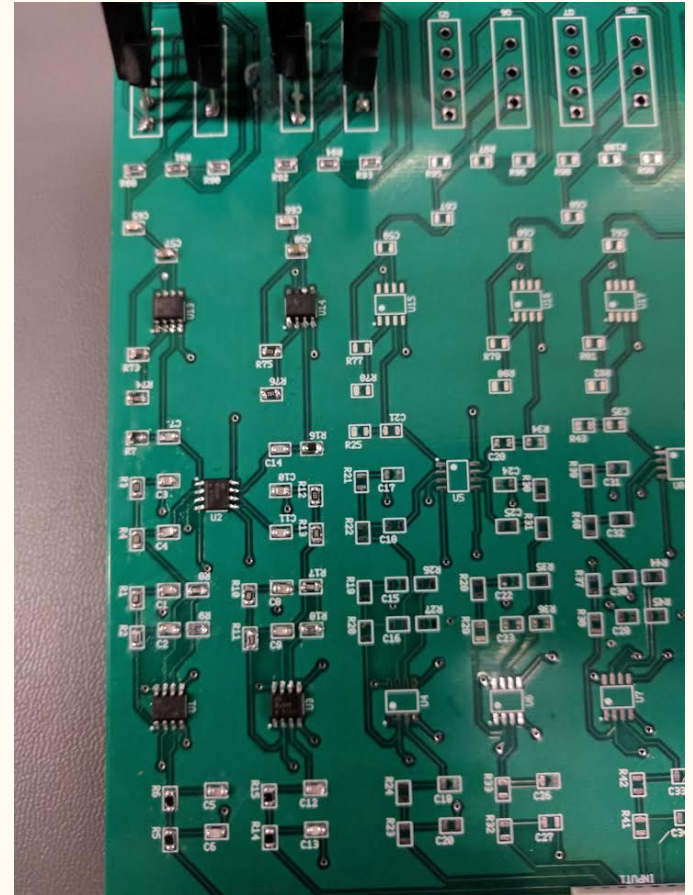
Results



< == Ground Plane

Two completed channels == >

< == Power Plane



Questions?

Budget

Spring 2016 Parts Order

Description	Digikey Part Number	Number Requested	Price Per Unit	Price
TI Launchpad	296-34797-ND	1	17.70	17.70
OP4584T OpAmp	296-23089-5-ND	4	15.01	60.04
ADA4891-3ARUZ OpAmp	ADA4891-3WARUZ-R7-ND	4	1.43	5.72
ADA4533 OpAmp	ADA4522-2ARZ-ND	4	4.31	17.24
			Total Cost: 100.70\$	

- Final expenditure amount with both parts and circuit board production was 492.95\$
- Initial budget was 300\$ but expected expenditure amount was considered flexible.
- Total amount spent over initial budget, 192.95\$
- Producing hardware while testing multiple iterations of parts and designs was not viable while maintaining 300\$ limit.

Total Spent - 492.95\$

Budget

Early Fallout 2016 Parts Order

Description	Digikey Part Number	Number Requested	Price Per Unit	Price
274Ohm Resistor	311-274CRCT-ND	18	0.021	0.38
100pF Capacitor	PCF1316CT-ND	27	0.3384	9.14
1500pF Capacitor	PCF1298CT-ND	25	0.3908	9.77
78.7Ohm Resistor	P78.7CCT-ND	10	0.10	1.00
1.43kOhm Resistor	311-1.43KRCT-ND	10	0.021	0.21
1000pF Capacitor	PCF1296CT-ND	18	0.3908	9.77
56.2Ohm Resistor	311-56.2CRCT-ND	10	0.021	0.21
2kOhm Resistor	311-2.00KRCT-ND	18	0.021	0.38
Surface Mount Test Points	36-5006-ND	10	0.316	3.16
1kOhm Resistor	311-1.0KARCT-ND	10	0.018	0.18
15kOhm Resistor	RMCF0805JT15K0CT-ND	10	0.017	0.17
100uF Capacitor	587-3978-1-ND	10	1.538	15.38
THS3001CD OpAmp	296-1762-5-ND	9	10.41	93.69
			Total Cost:	143.44\$

Final Fall 2016 Parts Order

Digi key Part Number	Number Requested	Price per unit	Price	Details
MJL1302AGOS-ND	8	3.50	28	PNP BJT
NJL3281DGOS-ND	8	4.59	36.72	NPN BJT
311-249CRCT-ND	10	0.021	0.21	249 Res
P4.99KCCT-ND	50	.022	1.10	4.99k Res
490-13311-1-ND	10	.165	1.65	.22uf cap
AD826ARZ-REELCT-ND	12	5.9480	71.38	AD826 OpAmp
311-1.37KRCT-ND	25	.01520	.038	1.37k Res
P365CCT-ND	10	.1	1.00	365 Res
311-7.68KRCT-ND	10	.021	0.21	7.68k Res
311-866CRCT-ND	10	.021	0.21	866 Res
311-5.76KRCT-ND	10	.021	0.21	5.76k Res
311-280CRCT-ND	10	.021	0.21	280 Res
RMCF0805JT10K0CT-ND	10	.017	0.17	10k Res
490-10741-1-ND	16	.0.106	1.70	200p Cap
399-9220-1-ND	10	.25	2.50	300p Cap
1276-1829-1-ND	25	.03960	0.99	20p Cap
490-1602-1-ND	10	0.117	1.17	130p Cap
A31118-ND	2	.5	1.00	Ribbon Cable Pins
			TOTAL COST (before tax): 148.81\$	